AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1. (currently amended) A multilayered integrated circuit comprising:

an upper conductive layer having upper conductive lines for carrying electrical signals among components of the integrated circuit;

a lower conductive layer having lower conductive lines for carrying electrical signals among components of the integrated circuit; and

an intermediate layer having conductive via holes electrically connecting the upper conductive lines with the lower conductive lines,

wherein

at least one line among either the upper conductive lines ~~and~~ or the lower conductive lines is an extraneous conductive line;

at least one via hole among the conductive via holes is an extraneous via hole;

the at least one extraneous conductive line is made of a material which is the same as the material of the upper and lower conductive lines; and

the at least one extraneous conductive line and extraneous via hole form an extraneous path, not connected to the operational functionality of the circuit, in order to confuse a reverse engineer. ~~performs functions which are unnecessary to the operation of the integrated circuit~~

2. (currently amended) The multilayered integrated circuit of claim 1, wherein the at least one extraneous conductive line has dimensions which are the same as the dimensions of the upper and lower conductive lines.

3. (original) The multilayered integrated circuit of claim 1, further comprising:

upper routing channels in which the upper conductive lines are placed; and

lower routing channels in which the lower conductive lines are placed,

wherein the at least one extraneous conductive line is placed in at least one of the routing channels.

4. (original) The multilayered integrated circuit of claim 1, wherein both the upper conductive lines and the lower conductive lines comprise extraneous conductive lines.

5. (original) The multilayered integrated circuit of claim 1, the integrated circuit being a CMOS integrated circuit.

6. (original) The multilayered integrated circuit of claim 1, the integrated circuit being a bipolar integrated circuit.

7. (original) The multilayered integrated circuit of claim 1, the integrated circuit being made of a III-V material.

8. (original) The multilayered integrated circuit of claim 1, wherein the at least one extraneous conductive line is a plurality of extraneous conductive lines.

9. (original) The multilayered integrated circuit of claim 8, wherein the plurality of extraneous conductive lines comprise extraneous conductive lines connected to a ground voltage.

10. (original) The multilayered integrated circuit of claim 8, wherein the plurality of extraneous conductive lines comprise extraneous conductive lines connected to a power supply voltage.

11. (original) The multilayered integrated circuit of claim 8, wherein the plurality of extraneous conductive lines comprise extraneous conductive lines connected to a clocked voltage.

12. (original) The multilayered integrated circuit of claim 1, further comprising additional conductive layers and additional intermediate layers between the additional conductive layers.

13. (currently amended) A process of making a multilayered integrated circuit comprising the steps of:

forming an upper conductive layer having upper conductive lines for carrying electrical signals among components of the integrated circuit;

forming a lower conductive layer having lower conductive lines for carrying electrical signals among components of the integrated circuit;

forming an intermediate layer having via holes electrically connecting the upper conductive lines with the lower conductive lines;

forming extraneous conductive lines in at least one conductive layer among the upper conductive layer and lower conductive layer, the extraneous conductive lines being made of a material which is the same of the material of the upper and lower conductive lines [[,]] ;

forming extraneous via holes among the via holes;

the extraneous conductive lines and extraneous via holes forming extraneous paths, not connected to the operational functionality of the circuit, in order to confuse a reverse engineer. ~~performing functions which are unnecessary to the operation of the integrated circuit~~

14. (currently amended) The process of claim 13, wherein the extraneous conductive lines have dimensions which are the same as the dimensions of the upper and lower conductive lines [[,]] .

15. (original) The process of claim 13, further comprising the steps of:

forming upper routing channels in which the upper conductive lines are placed;

forming lower routing channels in which the lower conductive lines are placed; and

placing the extraneous conductive lines in at least one of the routing channels.

16. (original) The process of claim 13, wherein the extraneous conductive lines are formed both in the upper conductive layer and lower conductive layer.

17. (original) The process of claim 13, wherein the integrated circuit is a CMOS integrated circuit.

18. (original) The process of claim 13, wherein the integrated circuit is a bipolar integrated circuit.

19. (original) The process of claim 13, wherein the integrated circuit is a circuit made of a III-V material.

20. (original) The process of claim 13, wherein the extraneous conductive lines comprise extraneous conductive lines connected to a ground voltage.

21. (original) The process of claim 13, wherein the extraneous conductive lines comprise extraneous conductive lines connected to a power supply voltage.

22. (original) The process of claim 13, wherein the extraneous conductive lines comprise extraneous conductive lines connected to a clocked voltage.

23. (currently amended) A method of designing a multilayered electronic circuit comprising functional conductive lines for transmission of electric signals and extraneous conductive lines, the designed multilayered circuit being suitable for making a corresponding three-dimensional multilayered electronic circuit, the method comprising:

providing a representation of a first conductive layer having first layer functional conductive lines for carrying electrical signals among components of the electronic circuit;

providing a representation of a second conductive layer having second layer functional conductive lines for carrying electrical signals among components of the electronic circuit;

providing a representation of functional via holes electrically connecting the first layer conductive lines with the second layer conductive lines; and

providing a representation of extraneous conductive lines to be inserted in at least one layer among the first conductive layer and the second conductive layer [[.]] ;

providing a representation of extraneous via holes electrically connecting the extraneous conductive lines, the extraneous conductive lines and extraneous via holes being designed to form an extraneous path, not connected to the operational functionality of the circuit, to confuse a reverse engineer.

24. (original) The method of claim 23, further comprising providing a representation of inserting the extraneous conductive lines in the first conductive layer and in the second conductive layer.

25. (original) The method of claim 24, further comprising providing a representation of cutting the extraneous conductive lines.

26. (original) The method of claim 25, wherein the extraneous conductive lines are cut according to multiple generations of random numbers.

27. (original) The method of claim 25, further comprising providing a representation of extraneous connection vias connecting extraneous conductive lines in the first layer to extraneous conductive lines in the second layer.

28. (original) The method of claim 27, wherein each extraneous conductive line has a first end and a second end, the method further comprising a computer generated representation of deleting extraneous connecting vias not located at the first end or the second end of an extraneous conductive line.

29. (original) The method of claim 25, wherein each extraneous conductive line has a first end and a second end, the method further comprising providing a representation of extraneous connection vias, located either at the first or at the second end of extraneous conductive lines.

30. (original) The method of claim 29, further comprising providing a representation of extraneous connecting vias, located between the first and the second end of extraneous conductive lines.

31. (original) The method of claim 23, further providing a representation of basic fill cells, each basic fill cell comprising at least one extraneous conductive line or at least one connecting via.

32. (original) The method of claim 31, further providing a representation of combining the basic fill cells to form larger cells.

33. (original) The method of claim 32, further comprising a representation of deleting portions of extraneous conductive lines, which portions are overlapping with the functional conductive lines.

34. (original) The method of claim 33, wherein the extraneous connecting vias have a first connecting end and a second connecting end, the method further comprising a representation of deleting extraneous connecting vias not connected to conductive lines at both the first connecting end and the second connecting end.

35. (original) The method of claim 34, further comprising a representation of deleting portions of extraneous conductive lines, which portions are close to the functional conductive lines.

36. (original) The method of claim 35, wherein the extraneous connecting vias have a first connecting end and a second connecting end, the method further comprising a

representation of deleting extraneous connecting vias not connected to conductive lines at both the first connecting end and the second connecting end.

37. (original) The method of claim 23, wherein each representation is a computer generated representation.

38. (currently amended) A process of making an electronic circuit comprising the steps of:

providing functional conductive lines for carrying electrical signals among components of the electronic circuit;

providing functional via holes for electrical connection of the functional conductive lines;

providing extraneous conductive lines, the extraneous conductive lines performing functions which are unnecessary to the operation of the electronic circuit ; and

providing extraneous via holes for electrical connection of the extraneous conductive lines , the extraneous conductive lines and extraneous via holes forming an extraneous path, not connected to the operational functionality of the circuit, in order to confuse a reverse engineer.

39. (original) The process of claim 38, wherein each extraneous conductive line has a first end and a second end, and wherein, in the step of providing extraneous via holes, the extraneous via holes are provided either at the first end or the second end of extraneous conductive lines.

40. (original) The process of claim 38, wherein the extraneous conductive lines and the extraneous via holes are combined to form basic fill cells.

41. (original) The process of claim 40, wherein the basic fill cells are combined to form larger cells.

42. (original) The process of claim 38, further comprising the step of deleting portions of the extraneous conductive lines overlapping with the functional conductive lines.

43. (original) The process of claim 38, wherein the extraneous via holes have a first connecting end and a second connecting end, the process further comprising the step of eliminating extraneous via holes not connected to conductive lines at both the first connecting end and the second connecting end.

44. (original) The process of claim 38, further comprising the step of eliminating portions of extraneous conductive lines, to maintain a predetermined minimum distance between extraneous conductive lines and functional conductive lines.

45. (new) The multilayered integrated circuit of claim 1, wherein the extraneous path is formed to carry a specious signal, unnecessary to the operation of the integrated circuit.

46. (new) The process of claim 13, wherein the extraneous paths carry specious signals, unnecessary to the operation of the integrated circuit.

47. (new) The method of claim 23, wherein the extraneous path is designed to carry a specious signal, unnecessary to the operation of the electronic circuit.

48. (new) The process of claim 38, wherein the extraneous path carries a specious signal, unnecessary to the operation of the electronic circuit.

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